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EXAMINER

ABRAHAM, ESAW T

ART UNIT PAPER NUMBER

2133

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/616,958

Applicant(s)

SLAVIN, KEITH R.

Examiner

Esaw T. Abraham

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-52 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-52 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

### **DETAILED ACTION**

1. The instant application having Application No. 10/616,958 has a total of 53 claims pending in the application. There are 6 independent claims and 47 dependent claims, all of which are ready for examination by the examiner.

### ***Drawings***

2. a) Figure 1B is objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: (see figure 1B, element 100).

b) Figure 5, element 508 is not leveled as described in the specification.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere CO.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims **1-53** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichiriu (U.S. PN: 7,002,823) in view of Hata et al. (U.S. PN: 6,842,359).

**As per claims 1, 29 and 31:**

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Ichiriu in figure 1 substantially disclose or teach a CAM device (100) includes a CAM array (101) (the CAM array includes a plurality of CAM cells arranged in rows for storing CAM words), error detector (107), priority encoder (114), comparand register (115) and read/write circuit (161). Instructions, addresses and commands are input to the CAM device via an instruction bus (IBUS) (145), address bus (ABUS) (141) and comparand bus (CBUS) (143). The CAM array also includes a validity storage (102) to store validity values and each validity value corresponds to a respective row of CAM cells and indicates whether the row contains a valid CAM word (each validity value may be represented by a single bit or multiple bits). Further, the CAM array (101) is coupled to comparand register (115) which also the comparand register (115) is used to store a comparand value received via the comparand bus (143), and outputs the comparand value to the CAM array (101) and during a compare operation, the comparand masked by a global mask value, then compared simultaneously with all the CAM words stored in the CAM array (101). Furthermore, each of the rows of CAM cells is coupled to a corresponding match line (182), and any match between the comparand and a valid CAM word results in a match signal being output to the priority encoder (114) and flag circuit (112) via the corresponding match line (182) (see col. 3, lines 29-67). **It is noted, however, Ichiriu does not explicitly teach** a circuit for pre-charging a match line between the CAM and the comparand as recited in claim 1. **On the other hand,** Hata et al. in FIG. 1 disclosed a CAM device (10) includes a CAM cell array (12), a search-bit line driver (14), a match detection circuit having a match line pre-charge circuit (16) and a match line sense circuit (18) (see col. 5, lines 51-58). In addition, Hata et al. teach that

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in the CAM device (10), for example, in the case of the CAM cell (24) shown in FIG. 2, the match line pre-charge circuit (16) pre-charges the match line ML to the high level at standby time. As a result of the search, if the n-bit data for one word completely matches the n-bit search-data individually, the match line ML remains at the high level, whereas if even one of the bits does not match, the line is discharged to the low level (see col. 6, lines 22-33). **It would have** been obvious to one of ordinary skill in the art at the time of the invention to combine the system of Ichiriu and the system of Hata et al. because they are in the same field of endeavor. **One of ordinary** skill in the art at the time of the invention would have been **motivated to do** so because the precharging circuit of Hata et al. would allow Ichiriu to achieve a reduction in power consumption and an increase in speed of CAM device encoding operation (see col. 3, lines 17-21 and col. 15, lines 22-32).

**As per claims 2-6:**

Most of the limitations of the claims 2-6 have been noted in the rejection of claim 1. In addition Ichiriu et al. teach that each of the CAM cells (201) in a given column is coupled to a pair of bit lines, BL (186 and BLB 187), and to a pair of comparand lines, (CL 184 and CLB 185) and each CAM cell (201) includes a memory cell to store at least one binary bit of data, and a compare circuit (XOR) to compare the content of the memory cell with a comparand signal and its complement presented on the comparand lines CL (184 and CLB 185). Each CAM cell 201 may further include a local mask cell to store a local mask value (such a CAM cell is referred to as a ternary CAM cell) (see col. 6, lines 33-60).

**As per claim 7:**

Most of the limitations of claim 7 have been noted in the rejection of claim 1. In addition Ichiriu et al. teach a CAM array 101 includes a plurality of CAM cells arranged in rows for storing CAM words and the CAM array also includes a validity storage (102) to store validity values (see col. 3, lines 44-49).

**As per claims 8-11:**

Most of the limitations of the claims (claims 8-11) have been noted in the rejection of claim 1. In addition Ichiriu et al. teach that each of the CAM cells (201) in a given column is coupled to a pair of bit lines, BL (186 and BLB 187), and to a pair of comparand lines, (CL 184 and CLB 185) and each CAM cell (201) includes a memory cell to store at least one binary bit of data, and a compare circuit (XOR) to compare the content of the memory cell with a comparand signal and its complement presented on the comparand lines CL (184 and CLB 185). Each CAM cell 201 may further include a local mask cell to store a local mask value (such a CAM cell is referred to as a ternary CAM cell) (see col. 6, lines 33-60).

**As per claims 12 and 13:**

These claims are at least rejected for their dependencies, directly or indirectly, on the rejected claim 1 above. They are therefore rejected as set forth above. In addition, Ichiriu teaches an error correction Code--CAM Device with Self-Correcting Function and thus far, error checking has been described primarily in terms of parity checking and in FIG. 16 illustrates an error detector (501) that operates on an error correction code stored with the CAM word instead of a parity bit. Error correction codes (e.g., Hamming

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codes) are sequences of bits formed, for example, by generating parity values for overlapping groups of bits within the CAM word and the chief advantage of error correction codes (ECCs) is that they permit location and therefore correction of a single bit error within a data value and further ECCs also permit detection of two-bit errors within a data value; errors that typically will not be detected by a parity-checking scheme because the two errors cancel one another insofar as they contribute to the even/odd parity of the data value (see col. 18, lines 4-39).

**As per claims 14-17 and 30:**

Ichiriu in figure 1 substantially disclose or teach a CAM device (100) includes a CAM array (101) whereby the CAM array includes a plurality of CAM cells arranged in rows for storing CAM words, error detector (107), priority encoder (114), comparand register (115) and read/write circuit (161). Instructions, addresses and commands are input to the CAM device via an instruction bus (IBUS) 145, address bus (ABUS) 141 and comparand bus (CBUS) 143, respectively. Further, the CAM array also includes a validity storage (102) to store validity values and each validity value corresponds to a respective row of CAM cells and indicates whether the row contains a valid CAM word (each validity value may be represented by a single bit or multiple bits). Ichiriu teaches that each CAM cell (201) may further include a local mask cell to store a local mask value (such a CAM cell is referred to as a ternary CAM cell) (see col. 6, lines 33-60). Furthermore, the CAM array (101) is coupled to comparand register (115) which also the comparand register (115) is used to store a comparand value received via the comparand bus (143), and outputs the comparand value to the CAM array (101) and

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during a compare operation, the comparand masked by a global mask value, then compared simultaneously with all the CAM words stored in the CAM array (101).

Furthermore, each of the rows of CAM cells is coupled to a corresponding match line 182, and any match between the comparand and a valid CAM word results in a match signal being output to the priority encoder (114) and flag circuit (112) via the corresponding match line (182) (see col. 3, lines 29-67). **It is noted, however, Ichiriu does not explicitly teach** a circuit for pre-charging a match line between the CAM and the comparand as recited in claim 1. **On the other hand,** Hata et al. in FIG. 1 disclosed a CAM device (10) includes a CAM cell array (12), a search-bit line driver (14), a match detection circuit having a match line pre-charge circuit (16) and a match line sense circuit (18) (see col. 5, lines 51-58). In addition, Hata et al. teach that in the CAM device (10), for example, in the case of the CAM cell (24) shown in FIG. 2, the match line pre-charge circuit (16) pre-charges the match line ML to the high level at standby time. As a result of the search, if the n-bit data for one word completely matches the n-bit search-data individually, the match line ML remains at the high level, whereas if even one of the bits does not match, the line is discharged to the low level (see col. 6, lines 22-33). **It would have** been obvious to one of ordinary skill in the art at the time of the invention to combine the system of Ichiriu and the system of Hata et al. because they are in the same field of endeavor. **One of ordinary** skill in the art at the time of the invention would have been **motivated to do** so because the precharging circuit of Hata et al. would allow Ichiriu to achieve a reduction in power consumption and an increase in

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speed of CAM device encoding operation (see col. 3, lines 17-21 and col. 15, lines 22-32).

**As per claims 18-22:**

Most of the limitations of the claims (claims 18-22) have been noted in the rejection of claim 14. In addition Ichiriu et al. teach that each of the CAM cells (201) in a given column is coupled to a pair of bit lines, BL (186 and BLB 187), and to a pair of comparand lines, (CL 184 and CLB 185) and each CAM cell (201) includes a memory cell to store at least one binary bit of data, and a compare circuit (XOR) to compare the content of the memory cell with a comparand signal and its complement presented on the comparand lines CL (184 and CLB 185). Each CAM cell 201 may further include a local mask cell to store a local mask value (such a CAM cell is referred to as a ternary CAM cell) (see col. 6, lines 33-60).

**As per claims 23-26:**

Most of the limitations of the claims (claims 23-26) have been noted in the rejection of claim 14. In addition Ichiriu et al. teach that each of the CAM cells (201) in a given column is coupled to a pair of bit lines, BL (186 and BLB 187), and to a pair of comparand lines, (CL 184 and CLB 185) and each CAM cell (201) includes a memory cell to store at least one binary bit of data, and a compare circuit (XOR) to compare the content of the memory cell with a comparand signal and its complement presented on the comparand lines CL (184 and CLB 185). Each CAM cell 201 may further include a local mask cell to store a local mask value (such a CAM cell is referred to as a ternary CAM cell) (see col. 6, lines 33-60).

**As per claims 32-35:**

Most of the limitations of the claims (claims 2-6) have been noted in the rejection of claim 31. In addition Ichiriu et al. teach that each of the CAM cells (201) in a given column is coupled to a pair of bit lines, BL (186 and BLB 187), and to a pair of comparand lines, (CL 184 and CLB 185) and each CAM cell (201) includes a memory cell to store at least one binary bit of data, and a compare circuit (XOR) to compare the content of the memory cell with a comparand signal and its complement presented on the comparand lines CL (184 and CLB 185). Each CAM cell 201 may further include a local mask cell to store a local mask value (such a CAM cell is referred to as a ternary CAM cell) (see col. 6, lines 33-60).

**As per claim 36:**

Most of the limitations of the claim (claim 36) have been noted in the rejection of claim 31. In addition, Ichiriu et al. teach a CAM array (101) includes a plurality of CAM cells arranged in rows for storing CAM words and the CAM array also includes a validity storage (102) to store validity values (see col. 3, lines 44-49).

**As per claims 37-40:**

Most of the limitations of the claims (claims 37-40) have been noted in the rejection of claim 31. In addition Ichiriu et al. teach that each of the CAM cells (201) in a given column is coupled to a pair of bit lines, BL (186 and BLB 187), and to a pair of comparand lines, (CL 184 and CLB 185) and each CAM cell (201) includes a memory cell to store at least one binary bit of data, and a compare circuit (XOR) to compare the content of the memory cell with a comparand signal and its complement presented on

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the comparand lines CL (184 and CLB 185). Each CAM cell 201 may further include a local mask cell to store a local mask value (such a CAM cell is referred to as a ternary CAM cell) (see col. 6, lines 33-60).

**As per claims 41 and 42:**

These claims are at least rejected for their dependencies, directly or indirectly, on the rejected claim 31 above. They are therefore rejected as set forth above. In addition, Ichiriu teaches an error correction Code--CAM Device with Self-Correcting Function and thus far, error checking has been described primarily in terms of parity checking and in FIG. 16 illustrates an error detector (501) that operates on an error correction code stored with the CAM word instead of a parity bit. Error correction codes (e.g., Hamming codes) are sequences of bits formed, for example, by generating parity values for overlapping groups of bits within the CAM word and the chief advantage of error correction codes (ECCs) is that they permit location and therefore correction of a single bit error within a data value and further ECCs also permit detection of two-bit errors within a data value; errors that typically will not be detected by a parity-checking scheme because the two errors cancel one another insofar as they contribute to the even/odd parity of the data value (see col. 18, lines 4-39).

**As per claims 43-46:**

Ichiriu in figure 1 substantially disclose or teach a CAM device (100) includes a CAM array (101) whereby the CAM array includes a plurality of CAM cells arranged in rows for storing CAM words, error detector (107), priority encoder (114), comparand register (115) and read/write circuit (161). Instructions, addresses and commands are

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input to the CAM device via an instruction bus (IBUS) (145), address bus (ABUS) (141) and comparand bus (CBUS) (143), respectively. The CAM array also includes a validity storage (102) to store validity values and each validity value corresponds to a respective row of CAM cells and indicates whether the row contains a valid CAM word (each validity value may be represented by a single bit or multiple bits). Ichiriu teaches that each CAM cell 201 may further include a local mask cell to store a local mask value (such a CAM cell is referred to as a ternary CAM cell) (see col. 6, lines 33-60). Further, the CAM array (101) is coupled to comparand register (115) which also the comparand register (115) is used to store a comparand value received via the comparand bus (143), and outputs the comparand value to the CAM array (101) and during a compare operation, the comparand masked by a global mask value, then compared simultaneously with all the CAM words stored in the CAM array (101). Furthermore, each of the rows of CAM cells is coupled to a corresponding match line 182, and any match between the comparand and a valid CAM word results in a match signal being output to the priority encoder (114) and flag circuit (112) via the corresponding match line (182) (see col. 3, lines 29-67). **It is noted, however, Ichiriu does not explicitly teach** a circuit for pre-charging a match line between the CAM and the comparand as recited in claim 1. **On the other hand,** Hata et al. in FIG. 1 disclosed a CAM device (10) includes a CAM cell array (12), a search-bit line driver (14), a match detection circuit having a match line pre-charge circuit (16) and a match line sense circuit (18) (see col. 5, lines 51-58). In addition, Hata et al. teach that in the CAM device (10), for example, in the case of the CAM cell (24) shown in FIG. 2, the match line pre-charge circuit (16)

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pre-charges the match line ML to the high level at standby time. As a result of the search, if the n-bit data for one word completely matches the n-bit search-data individually, the match line ML remains at the high level, whereas if even one of the bits does not match, the line is discharged to the low level (see col. 6, lines 22-33). **It would** have been obvious to one of ordinary skill in the art at the time of the invention to combine the system of Ichiriu and the system of Hata et al. because they are in the same field of endeavor. **One of ordinary** skill in the art at the time of the invention would have been **motivated to do** so because the precharging circuit of Hata et al. would allow Ichiriu to achieve a reduction in power consumption and an increase in speed of CAM device encoding operation (see col. 3, lines 17-21 and col. 15, lines 22-32).

**As per claims 47-52:**

Most of the limitations of the claims (claims 47-52) have been noted in the rejection of claim 43. In addition Ichiriu et al. teach that each of the CAM cells (201) in a given column is coupled to a pair of bit lines, BL (186 and BLB 187), and to a pair of comparand lines, (CL 184 and CLB 185) and each CAM cell (201) includes a memory cell to store at least one binary bit of data, and a compare circuit (XOR) to compare the content of the memory cell with a comparand signal and its complement presented on the comparand lines CL (184 and CLB 185). Each CAM cell 201 may further include a local mask cell to store a local mask value (such a CAM cell is referred to as a ternary CAM cell) (see col. 6, lines 33-60).

### **Conclusion**

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,975,526 Regev et al.

US PN: 6,944,710 Regev et al.

US PN: 7,017,089 Huse et al.

### **Status of Claims in the Application**

6. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i):

#### **Claims rejected in the Application**

Per the instant office action, claims 1-52 have received a first action on the merits and are subject of a first action non-final.

#### **Direction of Future Correspondences**

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

#### **Important Note**

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

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Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Esaw Abraham

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GUY LAMARRE  
PRIMARY EXAMINER